Fault-latch circuit protects switchers

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Many power-supply designers like to have a regulator latch off in the event of an overcurrent situation or other fault condition. Yet, many PWM controllers do not internally support this latch-off function. Most do, however, have a power-good output and an enable function. The circuit in **Figure 1** adds that latch-off capability at low cost in little additional space. The design is based on the LMS33460, which is a power-supply monitor in a tiny, five-lead SC-70 package. You just need to combine it with a few small passive parts, and the circuit is complete. When the Enable Input signal goes high, the voltage at the top of C_1 rises quickly to 5V. Because the output voltage is not yet alive, P_{GOOD} stays low, charging C_1 through R_1. Because the voltage on C_1 is zero at the instant of turn-on, Pin 5 of IC_1 pulls up to 5V and begins to drop at a time constant that C_1, R_1, and R_2 determine. If the output does not reach its normal operating voltage before the Pin 5 voltage drops to less than 3V, IC_1 pulls its output low and latches the regulator off.

If, however, the output comes into regulation before the latch times out, P_{GOOD} goes high and C_1 begins to discharge, raising the voltage on Pin 5 and keeping the supply enabled. R_2 provides a couple of volts to IC_1 to keep the IC alive in the event of a latch condition, and D_1 pulls down on the PWM's Enable when the system-enable command switches low. C_1 can be a small tantalum or ceramic capacitor. If you use a ceramic unit, choose a good dielectric, such as X5R. Also, the 5V supply's rising in less than 1 msec or so may eliminate the Enable, and the whole circuit simply runs from the 5V supply. **Figure 2** shows a normal start, and **Figure 3** shows start-up with the second output of a two-output regulator shorted. In both cases, the top trace is the system-enable signal, the second trace is IC_1's Pin 5, the third trace is the PWM Enable at IC_1's Pin 4, and the bottom trace is the regulator's output voltage. You can see in **Figure 3** that IC_1's Pin 5 decays to 3V, at which point it pulls the PWM Enable low, latching off the regulator.□

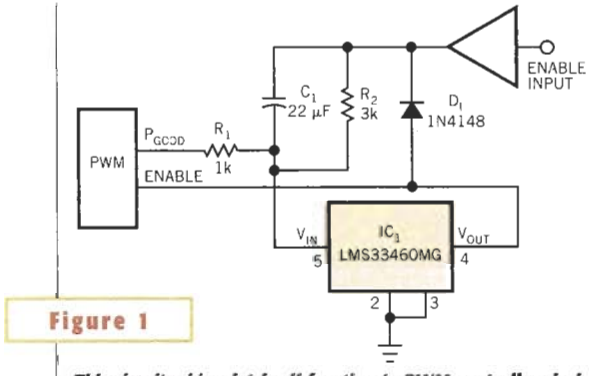

Figure 1 This circuit adds a latch-off function to PWM controllers lacking this feature.

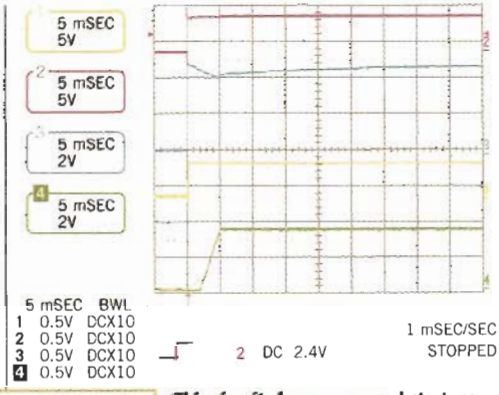

Figure 2 This circuit shows a normal start-up sequence for the circuit in Figure 1.

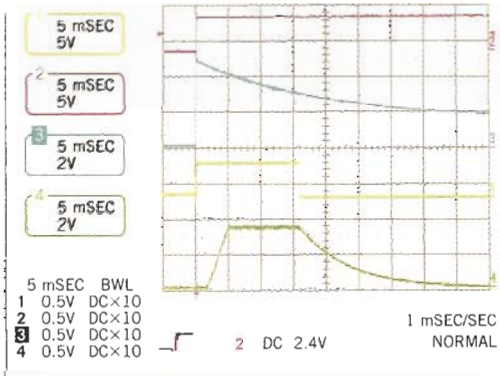

Figure 3 These traces represent start-up with the second output of a two-output regulator shorted.